IDEC Chip Design Contest

Neural recording circuits resilient to multi-channel variation

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Abstract

Record neural signals and send measurement data wirelessly is necessary to implement closed-loop neural stimulation systems. This work can achieve a dynamic range of more than 90dB by using delta-sigma structures and auto ranging structures in an integrated circuit (IC) chip. Various methods such as Bluetooth, inductive coil, and RF communication have been used for data transmission. However, these methods have problems that requiring a large area, limit movement and have a low data transmission rate relative to power. In this research, we adopted an optical communication technique for wireless data transmission from freely moving multiple experimental animals In this study, a noise calibration logic was also devised to reduce the mismatch of each channel. The designed IC chip size is 1mm2 in a standard 65nm CMOS process, consisting of 8 channels.

Design & Measurement

8CH neural signal sensor

The ADC used in the designed IC is a delta-sigma (DS) ADC, which has the advantage of shaping quantization noise into high frequencies through noise shaping. Therefore, the ADC noise performance in the low-frequency band we aim to measure is determined by the thermal noise of the integrator. The structure is designed to allow the noise calibration logic to change the amount of current used in the integrator ensuring a consistent overall noise level across channels in the system.

Auto-ranging digital prediction logics

To rapidly measure transient changes in neural signals, the Auto-ranging digital prediction was employed [1]. The digital prediction allows the modification of the range of variation by examining the sign (sign(ΔOut[n])) of the change in the output part of the signal. This adaptive adjustment of the quantizing range, different from traditional ADCs, enables the system to more rapidly and accurately measure momentary changes in neural signals by dynamically altering the quantizing range based on the signal's characteristics.

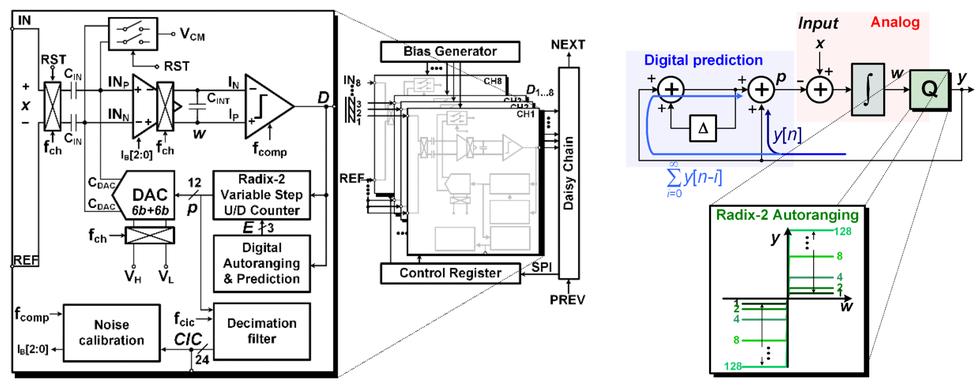

Figure 1. Recording stage block diagram

Resilient logic

The logic begins by shorting the initial input to VCM and then proceeds with the computation. It continuously sums the absolute differences of consecutive values of the CIC output to calculate the noise of ADC. After completing the noise adding and comparing it with the reference value predefined in the simulation, the logic determines whether to decrease or increase the current in the integrator. This design ensures that the noise variation in each channel is maintained at a similar level.

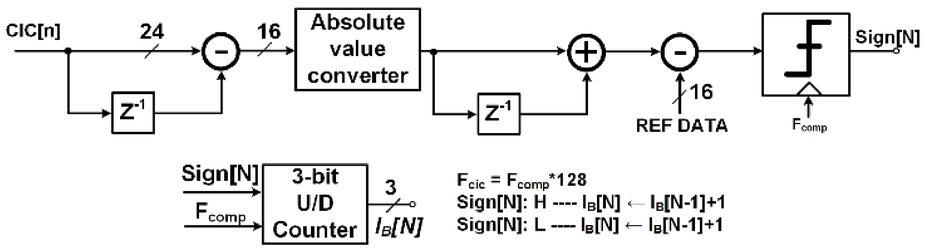

Figure 2. Resilient logic block diagram

Measurement

The left one shows FPGA connector part and the right one shows IC connector part. A 65-nm CMOS process was employed, and the total area occupied is 1mm^2. Each channel consists of an ADC, noise calibration block, and a CIC filter. The master clock and output data from the chip were managed using an FPGA (XEM6310). The chip's input signal was generated using APX526.

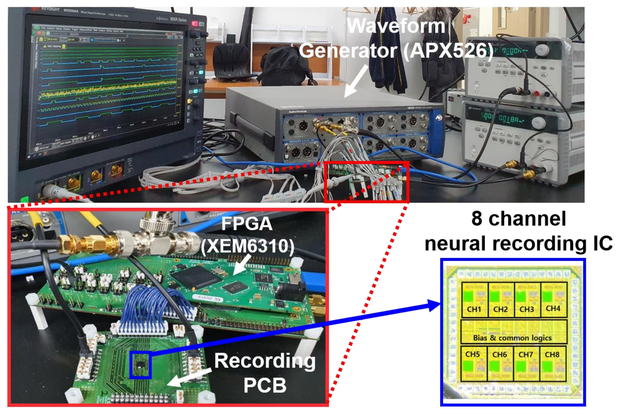

Figure 3. Measurement setup

Result & Conclusion

Result

Fig. 4. illustrates the Signal-to-Noise and Distortion Ratio (SNDR) of the ADC output before the CIC and after passing through the CIC filter for 10Hz input signals. The performance evaluation using measurements is shown in TABLE I. The overall system noise was determined by the thermal noise of the integrator, an increase in bias current would be expected to reduce the overall noise. However, noise is present regardless of the bias current. It is hypothesized that the system is not dominated by the integrator's noise but rather by Quantization noise or issues related to the differential non-linearity (DNL) of the bridge cap DAC used during the design. To address this, future designs will consider using a DAC in a form other than the bridge DAC.

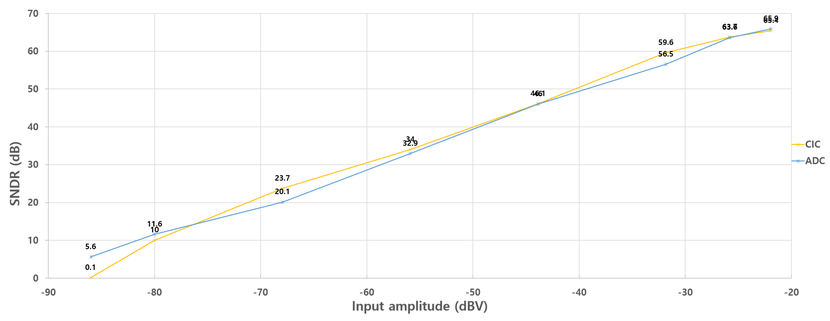

Figure 4. Output values SNDR according to various 10Hz input signal sizes.

TABLE I. Comparison Table

	[2]	[3]	[4]	This work
Power/CH (μW)	7.3	6	6.8	1.6
Supply (V)	1.2	0.8	1.2	1
Operation frequency (kHz)	400	320	1600	64
Noise density (nV/$\sqrt{Hz}$)	127	379	82	44.7
ENOB (bits)	14	8.8	11.3	10.6
Process (nm)	40	22	180	65

Conclusion

In this work, overall system could achieve less than 2μVrms input referred noise from 0.1Hz to 500Hz frequency range, rapidly record ~mV level of signal with PDA logics. Unfortunately, the designed noise calibration logic did not function properly due to increased noise flow caused by issues such as DAC mismatch

Reference

[1] C. Kim, et al. "Sub- μVrms-Noise Sub-μW/Channel ADC-Direct Neural Recording With 200mV/ms Transient Recovery Through Predictive Digital Autoranging," in IEEE Journal of Solid-State Circuits (2018)

[2] H. Chandrakumar, et al. “A 15.2-ENOB continuous-time ΔΣ ADC for a 200mVpp-linear-input-range neural recording front-end,” in IEEE ISSCC Dig. Tech. Papers, Feb. 2018.

[3] Yang, et al. "An AC-Coupled 1st-Order Δ-ΔΣ Readout IC for Area-Efficient Neural Signal Acquisition." IEEE Journal of Solid-State Circuits 58.4 (2023)

[4] Oh, et al. "Power-Efficient LFP-Adaptive Dynamic Zoom-and-Track Incremental ΔΣ Front-End for Dual-Band Subcortical Recordings." IEEE Transactions on Biomedical Circuits and Systems (2023).

Acknowledgement

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